IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 09/478,386, filed January 6, 2000, ~~pending~~now U.S. Patent 6,355,507, issued March 12, 2002, which is a divisional of application Serial No. 09/304,368, filed May 4, 1999, now U.S. Patent 6,204,095 ~~B1~~, issued March 20, 2001, which is a continuation of application Serial No. 09/056,124, filed April 6, 1998, now U.S. Patent 5,933,713, issued August 3, 1999.

Please replace paragraph number **[0002]** with the following rewritten paragraph:

[0002] Field of the Invention: The present invention relates to semiconductor devices and methods for fabricating semiconductor devices. More specifically, the invention relates to a method for packaging or encapsulating an ~~IC~~ integrated circuit (IC) die having conductive bumps or bonds that protrude beyond the IC covering or package.

Please replace paragraph number **[0012]** with the following rewritten paragraph:

[0012] According to the present invention, a method for forming a semiconductor device includes forming or providing a semiconductor wafer that has an integrated circuit or active surface defining a large plurality of integrated circuit die locations. As used herein, the term "wafer" includes traditional wafer ~~structures~~ structures, as well as silicon-on-insulator ~~(SDI)~~ (SOI), silicon-on-glass (SOG) and silicon-on-sapphire (SOS) substrates, among others known in the art. The active surface of the semiconductor wafer includes bond pads thereon for making external electrical connections. Conductive bumps or balls are formed on the bond pads. A top or outermost portion of each conductive bump is then planarized, that is, the top portion of each substantially spherical conductive bump is flattened to a common horizontal or vertical plane level. The exposed portions of the active surface of the semiconductor wafer (i.e., those parts not occupied by the conductive bumps) are filled with a layer of encapsulation material. The conductive bumps are then reformed or reshaped from a planarized shape to their preplanarized

shape (i.e., substantially spherical shape). The semiconductor wafer is then diced to form singulated semiconductor dice.

Please replace paragraph number **[0013]** with the following rewritten paragraph:

[0013] In addition to the aforementioned steps, a preferred method of the invention also includes singulating semiconductor dice and placing each singulated die in a mold to complete a second encapsulation step. This second encapsulation step comprises forming a layer of encapsulation material on the back and side surfaces of the semiconductor die in order to substantially or completely encapsulate the back and sides of each semiconductor die. The second encapsulation step can be accomplished either before or after the conductive bumps are reformed to their preplanarized shape, as described above. By combining the ~~previously-described~~ previously described method, wherein the active surface of each semiconductor die is filled with an encapsulation material, with the instant preferred methods, wherein the back and sides of each semiconductor die are covered with an encapsulant, a completely encapsulated chip scale package having raised conductive bumps thereon can be manufactured.

Please replace paragraph number **[0014]** with the following rewritten paragraph:

[0014] Another preferred method of the invention includes performing all of the previously described steps for forming conductive bumps on a semiconductor wafer and planarizing the top portion of each conductive bump thereon. The exposed portions of the active surface of the semiconductor wafer are filled with a layer of encapsulation material. The back surface of the semiconductor wafer opposing the active surface is then filled with a layer of encapsulation material to further protect the back surface of the semiconductor wafers. Finally, the conductive bond is reformed or reshaped from a planarized shape to its preplanarized shape (i.e., substantially spherical shape). The encapsulated semiconductor wafer is then diced to form singulated semiconductor dice. The reforming step can be conducted either before or after the back surface of the semiconductor wafer is layered with the ~~encapsulating~~ encapsulation material or, alternatively, before or after the semiconductor wafer is diced.

Please replace paragraph number **[0028]** with the following rewritten paragraph:

[0028] It is noted that any size of ball 30 may be ~~formed~~ formed, so long as the dimensions of the ball comply with design constraints of the final semiconductor device. For most applications, balls 30 will preferably have a diameter of from about 5 mil to about 15 mil. Because larger and smaller ball bond dimensions are envisioned for a variety of structures, other sized balls may be similarly manufactured. In this embodiment, it is desirable that the final height of balls 30 be greater than that of the ~~encapsulating~~ encapsulation material which will cover the active surface and surround the semiconductor device upon completion of the method of the present invention, as further described below.

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] By this planarizing step, balls 30 are flattened or planarized at their apices and widened so as to occupy a larger portion of the space overlying (but not necessarily connected to) active surface 22 of semiconductor substrate 20, thus forming planarized balls 40. A molten ~~encapsulating~~ encapsulation material is then injected under pressure as known in the art in a transfer-molding operation into the chamber defined between platen 36 and mold 32 to form a layer of encapsulant material 42 over the active surface 22 of semiconductor substrate 20. As can be observed in FIG. 4, encapsulant material layer 42 surrounds planarized balls 40, substantially covering the exposed portions of active surface 22. The thickness of encapsulant material layer 42 is preferably equal to or less than the height of planarized balls 40.

Please replace paragraph number **[0032]** with the following rewritten paragraph:

[0032] Once planarized balls 40 have been formed and active surface 22 has been covered with encapsulant material layer 42, platen 36 is detached from mold 32 and semiconductor substrate 20 is removed from the cavity of mold 32. Planarized balls 40 are once again heated and reflowed, as described in conjunction with FIG. 2, to form substantially spherical balls 30, as shown in FIG. 5. Planarized balls 40 can be reflowed by any of the

previously described means or by any other method for reflowing known in the art. Temperatures used to accomplish the reflowing of planarized balls 40 are necessarily dependent on the composition of the solder paste materials used. Heating times and temperatures must, however, be closely controlled to prevent decomposition of or damage to the semiconductor substrate 20, of any substructures thereon (e.g., bond pads 24 and integrated circuitry), and of the newly-formed encapsulant material layer 42. When reflowed, planarized balls 40 preferably coalesce to form substantially solid balls (i.e., conductive bumps) that are substantially free of surrounding small satellite balls.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] A second preferred fabrication process of the present invention includes fabricating the aforementioned semiconductor wafer according to the steps recited in conjunction with FIGS. 1 through 4. The semiconductor wafer resulting from the steps of FIGS. 1 through 4 is then singulated to form semiconductor die 51 (illustrated in FIG. 7), which includes planarized balls 40 and encapsulant material layer 42 overlying active surface 22. Semiconductor die 51 is placed into a second mold 38 and an ~~encapsulating~~ encapsulation material, preferably of the same composition as that of encapsulant material layer 42, is injected under pressure into second mold 38 to form a layer of encapsulant material 50 over side surfaces 46 and a back surface 48 of the semiconductor die 51. It is understood that encapsulant material 50 can also be different than encapsulant material layer 42 which was used to form a protective layer over active surface 22 of the semiconductor substrate 20. It is also understood ~~tha,~~ that, in actual practice, a large number of semiconductor dice 51 will be placed in cavities of a mold in a transfer-molding apparatus so that hundreds or thousands of semiconductor dice 51 will be covered with a layer of encapsulant material 50 over their side and back surfaces 46 and 48. As previously described with respect to encapsulation of the active surface 22 of a semiconductor substrate 20, transfer molding will be effected within chambers defined between a mold and a platen, or two cooperating mold sections, each chamber being appropriately vented as known in the art.

Please replace paragraph number **[0039]** with the following rewritten paragraph:

[0039] A fourth preferred fabrication process of the present invention includes forming the aforementioned semiconductor wafer according to the steps recited in conjunction with FIGS. 1 through 4. As shown in FIG. 9, the semiconductor wafer is placed into a second mold 38 and an ~~encapsulating~~ encapsulation material is injected, under pressure, into second mold 38 to form a layer of encapsulant material 56 over a back surface 54 of the semiconductor substrate. It is understood that encapsulant material layer 56 can be the same or different than encapsulant material layer 42 which was used to form a protective layer over active surface 22 of the semiconductor substrate 20.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

[0040] As depicted in FIG. 10, the semiconductor wafer is then removed from second mold 38 and singulated to form semiconductor die 58, which includes planarized balls 40 and encapsulant material layer 42. Planarized balls 40 are then reflowed to form substantially spherical balls 30 (i.e., conductive bumps), as shown in FIG. 11. Accomplishment of the instant fabrication process results in a partially encapsulated semiconductor die 58. Semiconductor die 58 includes encapsulant material layers 42 and 56 that substantially cover the exposed portions of active surface 22 and a back surface 54 of semiconductor die 58. As previously discussed, encapsulant material layers 42 and 56 can consist of the same or different materials.

Please replace paragraph number **[0044]** with the following rewritten paragraph:

[0044] A molten ~~encapsulating~~ encapsulation material is then injected, under pressure, into mold 32 to form a layer of encapsulant material 76 over the active surface 22 of semiconductor substrate 20. Encapsulant material layer 76 surrounds planarized balls 40, substantially covering the exposed portions of active surface 22. The thickness of encapsulant material layer 76 is preferably equal to or less than the height of planarized elastomer bond 72. As previously discussed above, any known encapsulant material can be used to form a protective layer over active surface 22.

Please replace paragraph number **[0045]** with the following rewritten paragraph:

[0045] Elastomer bumps 70 (i.e., conductive bumps) may be formed in any variety of suitable shapes and ~~sizes~~ sizes, so long as the dimensions of the bumps comply with design constraints of the final semiconductor device assembly. For most applications, elastomer bumps 70 will preferably have an average diameter of from about 5 mil to about 15 mil along a central portion thereof. Because larger and smaller elastomer bond dimensions are envisioned for a variety of structures, other sized bonds may be similarly manufactured. In this embodiment, it is desirable that the final size of elastomer bumps 70 be higher than encapsulant material layer 76 that surrounds the completed semiconductor device fabricated according to the instant method.

Please replace paragraph number **[0046]** with the following rewritten paragraph:

[0046] Once planarized elastomer bonds 72 have been formed and active surface 22 has been covered with encapsulant material layer 76, platen 36 is detached from mold 32 and semiconductor substrate 20 is removed from mold 32. Due to the inherent resilient characteristics of the elastomer material used, planarized elastomer bond 72 springs back to its precompressed shape (e.g., conical) upon removal of platen 36, as shown in FIG. 14. Where the structure from FIG. 14 comprises a semiconductor wafer, the wafer can be diced or segmented to create smaller, individual subsections of the semiconductor wafer, such as a semiconductor die 80 illustrated in FIG. 15. Semiconductor die 80 can be singulated by any process known to those skilled in the art.

Please replace paragraph number **[0047]** with the following rewritten paragraph:

[0047] Side surfaces 46 and back surface 48 of semiconductor die 80 can also be encapsulated by placing semiconductor die 80 into a second mold (such as second mold 38 in FIG. 7) and forming a layer of ~~encapsulating~~ encapsulant material on surfaces 46 and 48, as described above with reference to the various preferred process steps of the present invention.

Similarly, back surface 54 of the semiconductor substrate of FIG. 14 can be encapsulated according to the process steps described above in conjunction with FIG. 9.

Please replace paragraph number **[0049]** with the following rewritten paragraph:

[0049] A seventh preferred fabrication process of the present invention is depicted in FIGS. 18 and 19. The instant preferred fabrication process is initiated by forming conductive traces 102 on active surface 22 of semiconductor substrate 100 that contact bond pads 24 in order to repattern the configuration or layout of bond pads 24. Repatterning of the bond pads 24 is particularly useful when reconfiguring the layout of the bond pads on an existing semiconductor substrate to conform to a particular pattern on a carrier substrate, such as a PCB. Thereafter, the fabrication process steps described in conjunction with FIGS. 1 through 6 are performed, with the solder paste 28 being applied to that end of the conductive traces 102 opposite the end thereof attached to the bond pads 24. Execution of these steps results in a semiconductor ~~die~~ substrate 100 having an encapsulant material layer 42 that overlaps the conductive traces 102 on the active surface 22 of the semiconductor ~~die~~ substrate 100. The semiconductor ~~die~~ substrate 100 can be further encapsulated according to the process described in conjunction with FIGS. 7 and 8. It is understood that the present modification can be incorporated into the fabrication process depicted in conjunction with FIGS. 12 through 15 to produce a semiconductor die having elastomer bumps 70 thereon.